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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)		Application Number	10/579,766-Conf. #3580
		Filing Date	May 18, 2006
		First Named Inventor	Takamitsu Yamada
		Art Unit	2827
		Examiner Name	Not Yet Assigned
Sheet	1	of	1
		Attorney Docket Number	R2184.0495/P495

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	CA	TASIRAN et al.; "Linking Simulation with Formal Verification at a Higher Level"; Synergies for Design Verification; IEEE Design & Test of Computers; Vol. 21, No. 6; Jun 2004; pp. 472-482	
	CB	CHEN et al.; "Logic of Constraints: A Quantitative Performance and Functional Constraint Formalism"; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; Vol. 23, No. 8; August 2004; pp. 1243-1255	
	CC	DATTA et al.; "Assertion Based Verification Using HDVL"; Proceedings of the 17th International Conference on VLSI Design; Jan. 2004; pp. 319-325	
	CD	PIXLEY et al.; "Functional Verification 2003: Technology, Tools and Methodology"; Proceedings 5th International Conference, IEEE; Vol. 1; Oct. 2003; pp. 1-5	

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